REMARKS/ARGUMENTS

The Office Action mailed November 6, 2002 has been received and carefully considered. Claims 1- 12 are pending in the application, new claims 9-12 having been added by this Amendment.

At the outset, applicant notes that the Examiner has noted some items for correction. These corrections have been made. Specifically, Fig. 3, which was inadvertently omitted is provided with the proposed drawing corrections to Fig. 2. The postcard notes that 2 sheets of drawings were submitted. Clearly, Fig. 3 was the only drawing on sheet 2 as Figs. 1 and 2 were provided on sheet 1. Fig. 3 corrects the noted problem with page 5, lines 11 – 23 and the missing elements. Page 4, line 5 has been corrected to 1 μm; Fig. 2 has been corrected to include element 200 (a red-lined copy of Fig. 2 is attached with a request for correction); similarly for element 210 of Fig. 2; page 5 lines 4 – 6, the specification has been corrected so that the noted lines are now grammatically correct and make a sentence.

Claims 1 - 7 are rejected under 35 U.S.C. § 112, first paragraph as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make or use the invention. Claim 1 has been amended to overcome the 35 U.S.C. § 112, first paragraph rejection by deleting the reference to any circuitry between the image sensor and the edges of the image sensor.

Claims 1 – 7 are further rejected under 35 U.S.C. § 103 (a) as being unpatentable over Sayag et al. (U.S. Patent No. 5,510,623, herein after "Sayag") in view of Gowda et al. (U.S. Patent No. 6,115,066, herein after "Gowda"). Claim 8 is rejected under 35 U.S.C. § 103 (a) as being unpatentable over Sayag in view of Gowda in further view of Kawahara et al. (U.S. Patent No. 5,321,303, hereinafter "Kawahara") and in further view of Stettner et al. (U.S. Patent No. 5,629,524, hereinafter "Stettner"). These rejections are respectfully traversed.

Sayag describes a CCD image sensor array having a centrally disposed

photosensitive readout register thus creating a CCD image sensor having two halves. At col. 3 lines 6, - 15, Sayag specifies chamfered corners avoiding the use of an "amplifier corner". Gowda merely indicates that CMOS imagers are inherently lower cost than CCD devices.

In contrast, as recited in Claim 1 (as amended) as follows:

> 1. (Amended) A CMOS image sensor circuit, comprising:
>
> a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of rows and columns, and image sensor logic on said substrate, said logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor other than said rows individually,
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> said substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge,
>
> said image sensor extending between said first edge, said second edge, and said third edge, such that a first area adjacent said first edge of the chip includes first pixels of the image sensor, a second area adjacent said second edge of the chip includes image sensors, and a third area adjacent said third edge of the chip includes image sensors,
>
> said row logic being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor;
>
> a pixel interpolator and said chip driver circuitry located between said image area and said fourth edge; and
>
> a second CMOS image sensor substrate configured similarly to said first CMOS image sensor substrate and abutted to one of said edges of said first CMOS image sensor substrate. (emphasis added)

The present invention is directed towards image sensors that have row logic inside an image sensor and have chip drivers and pixel interpolator along a fourth edge of the image sensor. At least two CMOS image sensors are butted to each other. That is, the image sensor circuit of the present invention is formed from at least two image sensors that are butted to each other and missing pixels and image loss at the butted edges are corrected using pixel interpolation. Each of the image sensors has chip driver circuitry and pixel

interpolation circuitry. The image sensor of Sayag has chamfered corners. Sayag's image sensors are not butted nor are they buttable without substantial image loss at the corners of Sayag's image sensor nor is there any teaching that image sensors are buttable. Further, Sayag corrects for image loss at the photosensitive readout register area by multiplying the pixels of the photosensitive readout register area by a constant to match the other pixels (see col. 7, lines 6 – 8). Sayag does not perform pixel interpolation. Sayag doe not have a pixel interpolator located between the image area and the fourth edge of the image sensor.

Sayag does not include each and every feature of the present invention as recited in claim 1. Gowda merely describes the use of CMOS imagers because of their inherently lower cost and adds nothing else to fill in those features and elements of the present invention that are not described by Sayag. Neither Sayag nor Gowda alone or in combination teach or disclose each and every feature of the present invention as recited in Claim 1.

Kawahara describes a plurality of semiconductor chips "connected together to form a continuous or elongated line sensor" with the "higher the resolving power, the smaller the distance between each pair of adjacent sensors" (see Kawahara col. 1, lines 13 – 16 and col. 1, line 67 – col. 2, line1). Stettner describes a large format High-Speed Crystallography Detector (HSCD) formed of detector chip arrays arranged three dimensionally on top of readout arrays chips and connected to drive and output electronics via a cable (see col. 4, lines 40 – 63). Further, Stettner states at col. 4, lines 57 – 60, that "a three-dimensional hybrid configuration is necessary to minimize regions as seen from above on the area sensor that have few or no detectors".

Sayag and Gowda have already been discussed above and fail to teach each and every feature of claim 8. Kawahara describes the formation of an elongated (linear) line sensor. Neither Kawahara nor Stettner over come the deficiencies as noted above with respect to Sayag and Gowda. That is, Stettner neither describes nor provides for any correction of any missing pixel data either on any of the image sensors used to form the HSCD or connected by any means thereto. Further, Stettner requires a three-dimensional

configuration in order to minimize areas which would be missing detectors and, therefore, require pixel correction. Kawahara is also silent on the issue of pixel interpolation. Neither Sayag, nor Gowda, nor Kawahara nor Stettner alone or in any combination teach or disclose each and every feature of the present invention as recited in Claim 8.

Moreoever, Sayag is directed towards a CCD image sensor with a centrally disposed photosensitive readout register. Sayag's image sensor has chamfered corners which prohibits the image sensors of Sayag from being abutted. Sayag's image sensor has no pixel interpolator located between the image area and a fourth edge. Gowda is directed towards a CMOS image sensor with direct digital correlated double sampling. Sayag and Gwoda are each directed toward different problems and there is, thus, no motivation to combine the references. Not only is there no motivation to combine Sayag and Gowda, neither Sayag nor Gowda address the problem of the present invention, which is to form large format image sensor by abutting a plurality of image sensors each having row logic in an inside area between image areas. The Office Action is combining the references in hindsight only to reject the claims of the present invention.

It is, therefore, submitted that Claim 1 is patentable over the art of record for at least the above reasons. Claims 2 – 7 depend directly or indirectly from Claim 1 so are also submitted to be patentable over the art of record. It is also, submitted that Claims 8 is patentable over the art of record for at least the above reasons. It is submitted that newly added claims 9 – 12 are patentable over the art of record for at least the above reasons.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made in the Specification

The paragraph beginning on page 4, line 3, and ending on page 4, line 5.

There can be a small space 107 between the two adjacent chips 106, 109 due to the roughness of the edges. The small space is typically of the order of 1μm.

The paragraph beginning on page 5, line 4, and ending on page 5, line 10.

Hence, the pixels 204 are [those] adjacent pixels 202 [or] separated by a space that is preferably less than one – two pixels wide including guard rings 103, 208 and space 210. The array of image sensors 99 therefore forms a system where each pixel is separated from each adjacent pixel in the adjacent image sensor by an amount that is small enough to allow interpolation of the missing space, to thereby obtain an uninterrupted image.

The paragraph beginning on page 5, line 15, and ending on page 5, line 23.

SRAM 304 stores temporary results, and also buffers the information as needed. Connections 306 can couple commands to the row circuitry. The overall chip driver 310 can be the same as conventional, including A/D converters for each column and the like. Element 312 also preferably includes a two-pixel interpolator that is used to interpolate for the missing pixels at areas 105 and 107 and includes pixel interpolation at space 210 caused by rough edges of the butted image sensors. Pixel interpolation is well known in the art, and is described, for example, in US Patent no. 4,816,923. More preferably, the pixel interpolation is done in software.

Version With Markings to Show Changes Made in the Claims

1. (Amended) A CMOS image sensor circuit, comprising:

a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of rows and columns, and image sensor logic on said substrate, said logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor other than said rows individually,

said substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge,

said image sensor extending between said first edge, said second edge, and said third edge, [with no circuitry being located between said image sensor and any of said first, second or third edges,] such that a first area adjacent said first edge of the chip includes first pixels of the image sensor, a second area adjacent said second edge of the chip includes image sensors, and a third area adjacent said third edge of the chip includes image sensors,

said row logic being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor[.];

a pixel interpolator and said chip driver circuitry located between said image area and said fourth edge; and

a second CMOS image sensor substrate configured similarly to said first CMOS image sensor substrate and abutted to one of said edges of said first CMOS image sensor substrate.